



UNITED STATES PATENT AND TRADEMARK OFFICE

Cen

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/782,455

02/19/2004

Michael Aaron Kaply

AUS920031049US1(4037)

5175

45557

7590

01/12/2007

IBM CORPORATION (JSS)

C/O SCHUBERT OSTERRIEDER & NICKELSON PLLC

6013 CANNON MOUNTAIN DRIVE, S14

AUSTIN, TX 78749

EXAMINER

ESTRADA, ANGEL R

ART UNIT

PAPER NUMBER

2831

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
----------------------------------------	-----------	---------------

3 MONTHS

01/12/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/782,455

Applicant(s)

KAPLY ET AL.

Examiner

Angel R. Estrada

Art Unit

2831

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 33-60 is/are pending in the application.
- 4a) Of the above claim(s) 45-52 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 33,34,37-41,43,44 and 53-60 is/are rejected.
- 7) ☒ Claim(s) 35,36 and 42 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 33, 34, 37-41, 43, 44 and 53-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata (US 6,600,658).

Regarding claim 33, Iwata discloses an enclosure (see figure 1) for an electronic device, the enclosure comprising: an interior surface and an outside surface of the enclosure (see figure 1), the interior surface (see figure 1) enclosing the electronic device; mounting sites (5) to mount integrated circuit, wherein the mounting sites couple with the interior surface; a pattern of interconnects (6) coupled with the interior surface and interconnected with the mounting sites to transmit signals between the integrated circuits (see figure 1); and at least one switch (16 or 12 or 13) coupled with the pattern of interconnects at the interior surface and exposed via the outside surface of the enclosure to receive input from outside of the enclosure (see figure 2).

Regarding claim 34, Iwata discloses the enclosure (see figure 1), further comprising other components coupled (16 or 12 or 13) with the pattern of interconnects via the mounting sites (see figure 1).

Regarding claim 37, Iwata discloses the enclosure (see figure 1), wherein the pattern of interconnects (6) comprises a conductive paint applied directly to the enclosure (see figure 1), wherein the enclosure is composed of a substantially non-conductive plastic (see figure 2, notice the cross section hatching it resembles a plastic material).

Regarding claim 38, Iwata discloses the enclosure (see figure 1), wherein the enclosure (see figure 2) is composed of a pliable material (see figure 2, notice the cross section hatching it resembles a plastic material).

Regarding claim 39, Iwata discloses the enclosure (see figure 1), wherein the pattern of interconnects (6) is coupled with the enclosure via at least one layer of non-conductive laminates (see figure 1).

Regarding claim 40, Iwata discloses the enclosure (see figure 1), wherein the pattern of interconnects (6) applied to an interior surface of the enclosure comprises a layer of metal having portions etched away to reveal the pattern of interconnects (see figure 1).

Regarding claim 41, Iwata discloses a system (see figure 1) comprising: an enclosure comprising an interior surface and an outside surface (see figure 1), the interior surface enclosing an electronic device (see figure 1); integrated circuits; mounts in the enclosure to mount the integrated circuits (see figure 1), wherein the mounts couple with the interior surface; a pattern of interconnects (6) coupled with the interior surface and interconnected with the mounts to transmit signals between the integrated circuits (see figure 1); and at least one switch (16 or 12 or 13) coupled with the pattern

of interconnects (6) and exposed via the outside surface of the enclosure to receive input from outside of the system (see figure 1).

Regarding claim 43, Iwata discloses the system (see figure 1), wherein the pattern of interconnects (6) resides on a laminate, the laminate being adhered to the interior surface of the enclosure (see figure.1).

Regarding claim 44, Iwata discloses the system (see figure 1), wherein the pattern of interconnects (6) is coupled with a circuit board internal of the enclosure to communicatively couple the integrated circuits with other components mounted to the circuit board (see figure 1).

Regarding claim 53, Iwata discloses an apparatus (see figure 1) comprising: an enclosure comprising an interior surface to enclose a device and an outside surface exposed to the exterior of the enclosure (see figure 1); and the device comprising a mounting site (5) to mount an integrated circuit, wherein the mounting site is on the interior surface, and a pattern of interconnects (6) on the interior surface, wherein the pattern of interconnects (6) is coupled with the mounting site to transmit signals for the integrated circuit (see figure 1).

Regarding claim 54, Iwata discloses the apparatus (see figure 1), further comprising a circuit board (see figure 1) within the enclosure and interconnected with the pattern of interconnects (6).

Regarding claim 55, Iwata discloses the apparatus (see figure 1), further comprising at least one component (16 or 12 or 13) located on the outside surface and coupled with the pattern of interconnects (6) directly through the enclosure (see figure 1).

Regarding claim 56, Iwata discloses the apparatus (see figure 1), further comprising the integrated circuit coupled with the mount (see figure 1).

Regarding claim 57, Iwata discloses the apparatus (see figure 1), wherein the pattern of interconnects (6) of the device is coupled with part of the enclosure (see figure 1).

Regarding claim 58, Iwata discloses the apparatus (see figure 1), wherein the part of the enclosure is composed of a non-conductive material (see figure 2, notice the cross section hatching it resembles a plastic material).

Regarding claim 59, Iwata discloses the apparatus (see figure 1), wherein the part of the enclosure is to insulate independent paths of the pattern of interconnects (see figure 1).

Regarding claim 60, Iwata discloses the apparatus (see figure 1), wherein the part of the enclosure is a plastic (see figure 2, notice the cross section hatching it resembles a plastic material).

Allowable Subject Matter

2. Claims 35, 36 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: The primary reasons for the indication of the allowability of claims 35, 36 and 42 are:

Regarding claim 35, the prior art does not teach or fairly suggest in combination with the other claimed limitations an enclosure, wherein the at least one switch

comprises an optical switch to toggle in response to a change in light sensed by the optical switch.

Regarding claim 36, the prior art does not teach or fairly suggest in combination with the other claimed limitations an enclosure, wherein the at least one switch comprises a pressure-sensitive switch coupled with the pattern of interconnects via one of the mounts.

Regarding claim 42, the prior art does not teach or fairly suggest in combination with the other claimed limitations a system comprising sensors to sense environmental conditions, the sensors being oriented to face the exterior of the enclosure.

These limitations are found in claims 35, 36 and 42, and are neither disclosed nor taught by the prior art of record, alone or in combination.

Response to Arguments

3. Applicant's arguments with respect to claims 33-44 and 53-60 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication should be directed to Angel R. Estrada at telephone number (571) 272-1973. The Examiner can normally be reached on Monday-Friday (8:30 -5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272-2800 Ext: 31. The fax phone

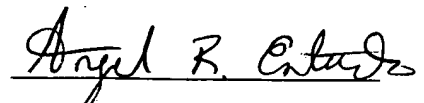
Art Unit: 2831

number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 19, 2006



Angel R. Estrada
Primary Examiner
Art Unit: 2831